REMARKS/ARGUMENTS

Claims 1-23 were pending in the present application. By virtue of this response, no claims have been cancelled, claims 1, 8, 14 and 19-23 have been amended, and new claims 24-33 have been added. Accordingly, claims 1-33 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

Double Patenting

Claims 8-13 and 19-23 are provisionally rejected as allegedly being unpatentable under the doctrine of judicially created double patenting over claims 1-6 and 8 of U.S. Patent Application Serial No. 10/846875 to Morikawa et al. in view of Larson et al. (US 5,537,350).

With this communication Applicant has amended claim 8 to recite a memory structure comprising at least a plurality of sidewall memory transistors. Each sidewall memory transistor comprises only a single gate electrode, a channel region, a pair of diffusion regions formed on both sides of the channel region and a pair of memory functional units formed on both sides of the gate electrode wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. Support for this amendment can be found in the specification at page 24, lines 23-24, page 25, lines 15-16 and page 33, line 17 through page 38, line 16.

Nowhere do claims 1-6 and 8 of Morikawa et al. disclose a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode that can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. Neither does Larsen et al. anywhere disclose this element. Accordingly, claim 8 cannot be rendered obvious by claims 1-6 and 8 of Morikawa et al. in view of Larsen et al. and Applicant respectfully requests withdrawal of this rejection.

Claims 9-13 each depend from amended claim 8. Accordingly, claims 9-13 cannot be rendered obvious by claims 1-6 and 8 of Morikawa et al. in view of Larsen et al. and Applicant respectfully requests withdrawal of this rejection.

With this communication, claim 19 has been amended to recite a memory structure comprising at least a plurality of sidewall memory transistors. Each sidewall memory transistor comprises only a single gate electrode, a channel region, a pair of diffusion regions formed on both sides of the channel region and a pair of memory functional units formed on both sides of the gate electrode wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode.

Accordingly, for the reasons discussed above with respect to claim 8, amended claim 19 cannot be rendered obvious by Morikawa et al. in view of Larsen et al. and Applicant respectfully requests withdrawal of this rejection.

Additionally, claims 20-23 are each dependent on amended claim 19. Accordingly, claims 20-23 cannot be rendered obvious by claims 1-6 and 8 of Morikawa et al. in view of Larsen et al. and Applicant respectfully requests withdrawal of this rejection.

Rejections under 35 U.S.C. § 102

Claims 8-11 and 19-21 are rejected as allegedly being anticipated by Kamei et al. (US2003/0164517).

As discussed above, with this communication Applicant has amended claims 8 and 19 to recite a memory structure comprising a plurality of sidewall memory transistors. Each sidewall memory transistor comprises only a single gate electrode, a channel region, a pair of diffusion regions formed on both sides of the channel region and a pair of memory functional units formed on both sides of the gate electrode.

Kamei et al. discloses a memory structure having memory cells that include three gate electrodes (104, 106A and 106B in Figure 1). As noted above, however, amended claim 8 recites a memory transistors each including only a single gate electrode. Accordingly, the structure disclosed by Kamei et al. is different from that recited in amended claims 8 and 19. Thus, Kamei et al. cannot anticipate amended claims 8 and 19 and Applicant respectfully requests withdrawal of this rejection.

Claims 9-11 depend from amended claims 8 and claims 20-23 depend from amended claim 19. Accordingly, Kamei et al. cannot anticipate claims 9-11 and 20-23 and Applicant respectfully requests withdrawal of this rejection.

Rejections under 35 U.S.C. § 103

Claims 1-23 are rejected as allegedly being unpatentable over Larsen et al. in view of Sakagami et al. (5,838,041).

With this communication claims 8 and 19 have been amended to recite a memory (claim 8) or storage (claim 19) structure comprising at least a plurality of sidewall memory transistors. Each sidewall memory transistor comprises only a single gate electrode, a channel region, a pair of

diffusion regions formed on both sides of the channel region and a pair of memory functional units formed on both sides of the gate electrode wherein a writing or erasing operation to a selected one of either of the memory functional elements formed on both sides of the gate electrode can be executed independently from the other unselected memory functional element by controlling each voltage applied to the diffusion regions and the gate electrode. Additionally, claims 1 and 14 have been amended to recite computer systems including the same elements.

Sakagami et al. discloses a semiconductor memory device having source/drain regions with a gate electrode interposed therebetween. Charge carrier accumulation layers are formed at side walls of the gate electrode. (Sakagami et al.: col. 4, lines 6-25; Fig. 2.) Sakagami et al. discloses one embodiment in which the charge carrier accumulation layer is formed on the drain side of the gate electrode and a second embodiment in which the charge carrier accumulation layer is formed on the source side. (Sakagami et al.: col. 7, lines 23-35; col. 8, line 38--col. 9, line 35; Figs. 8A, 8B, 12A and 12B.)

Nowhere, however, does Sakagami et al. disclose that a writing or erasing operation to a selected one of *either* of the memory functional elements formed on both sides of the gate electrode can be executed independently, as recited by amended claims 1, 8, 14 and 19. Indeed, in the memory device of Sakagami et al., it would be difficult to write or delete data in the right sidewall area of the gate electrode because the N-diffusion layer 16 extends to the area under gate electrode 13, making it difficult to inject charge into the right side wall area. And, as noted above, Larsen et al. does not disclose this element. Accordingly, claims 1, 8, 14 and 19 cannot be rendered obvious by either Sakagami et al., Larsen et al. or any hypothetical combination of the two references and Applicant respectfully requests withdrawal of this rejection.

Claims 2-7 depend from claim 1, claims 9-13 depend from claim 8, claims 15-18 depend from claim 14 and claims 20-23 depend from claim 19. Accordingly, claims 2-7, 9-13, 15-18 and 20-23 cannot be rendered obvious by either Sakagami et al., Larsen et al. or any hypothetical combination of the two references and Applicant respectfully requests withdrawal of this rejection.

With this communication, Applicant has added new claims 24-33. Support for new claims 24 and 29 can be found in the specification at page 20, lines 21-22. Support for new claims 25 and 30 can be found in the specification at page 43, lines 23 through page 44 line 1. Support for new claims 26 and 31 can be found in the specification at page 44, lines 6-8 and page 45 lines 11-13. Support for new claims 27 and 32 can be found in Figure 11. Support for new claims 28 and 33 can be found in the specification at page 15, line 24 through page 16, line 24.

CONCLUSION

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 259052004500. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: February 9, 2006

Respectfully submitted,

By_____

Douglas G. Hodder
Registration No.: 41,840
MORRISON & FOERSTER LLP
755 Page Mill Road
Palo Alto, California 94304-1018
(650) 813-4203